WHAT IS CLAIMED IS:

1. A processor operable from an M-bit instruction set or an N-bit instruction set, where M and N are integers, and M is less than N, comprising:

a memory unit for storing at least first and second instruction streams respectively comprising N-bit instructions and M-bit instructions

an execution unit operable to receive execution signals to execute the N-bit instructions;

a decode unit coupled to the memory unit and to the execution unit to receive and decode the first and second instruction streams from the memory unit to produce therefrom the execution signals, the decode unit including a translation unit for receiving each of the M-bit instructions to translate each of a first group of the M-bit instructions to a corresponding one of the N-bit instructions, and to translate each of a second group of the M-bit instructions to two or more N-bit instructions for decoding by the decode unit.

2. The processor of claim 1, wherein each of the M-bit and N-bit instructions are stored in the memory unit at locations identified by memory addresses having at least one bit position set to a first state to identify a memory address of an M-bit instruction and a second state to identify a memory address of an N-bit instruction.

3. The processor of claim 2, the N-bit instruction stream including at least one N-bit branch instruction, the decode unit operating to execute the N-bit branch instruction to switch from executing N-bit instructions to executing M-bit instructions.

4. The processor of claim 1, where N is equal to 2M.

5. The processor of claim 1, wherein M is 16 and N is 32.

6. The processor of claim 2, wherein the one bit position is the least significant bit of the memory address.

7. A processor unit, including

a memory for storing a plurality of instructions, including M-bit instructions and N-bit instructions where M and N are integers and M is less than

N, each instruction being stored at a memory location identified by a memory address, each memory address having a bit position set to a first state for M-bit instructions and to a second state for N-bit instructions;

an instruction flow control unit for retrieving the instructions from the memory for controlling execution of the retrieved instructions, the instruction flow control unit including a translation unit operable to receive ones of the M-bit instruction for translation to a sequence of two or more N-bit instructions.

8. A microprocessor, comprising:

a memory element containing a plurality of M-bit instructions and N-bit instructions where M and N are integers and M is less than N;

an instruction fetch unit coupled to the memory element for retrieving selected ones of the M-bit instructions or N-bit instructions therefrom, the instruction fetch unit including,

a translator unit for translating each of the M-bit instructions fetched from the memory element into a sequence of one or more N-bit instructions; and

a decode unit coupled to the memory element and to the translator unit for receiving each of N-bit instructions fetch from the memory element and each of N-bit instructions from the translator unit for decoding such N-bit instructions.

9. The microprocessor of claim 8, including at least one target register for holding a target address, the plurality of N-bit instructions including a prepare target instruction that, when executed by the microprocessor, loads the target address in the target register.

10. The microprocessor of claim 9, wherein the plurality of N-bit instructions includes a BLINK branch instruction operating to use the target address in the target register to branch to cause an M-bit target instruction or an N-bit target instruction to be fetched from the memory element for translation or decode, respectively.

11. The microprocessor of claim 10, wherein the BLINK branch instruction is an unconditional branch instruction.

12. The microprocessor of claim 9, wherein the target address includes a bit position set to a first state to identify an M-bit target instruction.

13. The microprocessor of claim 12, wherein the bit position is set to a second state to identify an N-bit target instruction.

14. A microcomputer formed on single chip, including

memory storing M-bit instructions and N-bit instructions where M and N are integers, and N is greater than M;

a translator coupled to the memory to receive M-bit instructions for translation of each received M-bit instruction to a sequence of one or more N-bit instructions; and

a decoder coupled to the memory and to the decoder for receiving and decoding the N-bit instructions.

15. The microcomputer of claim 14, wherein M is 16 and N is 32.

16. The microcomputer of claim 14, where the N-bit instructions include an N-bit branch instruction that contains data indicative of a branch address of a target instruction, the branch address having a bit position set to a first state when the target instruction is an M-bit instruction.

17. A method of executing M -bit instructions and N-bit instructions by a microcomputer formed on a single chip, M and N being integers, and M is less than N, the method including the steps of:

storing the M-bit and N-bit instructions in a memory;

operating in a first mode to sequentially decode ones of the N-bit instructions;

operating in a second mode to sequentially translate ones of the M-bit instructions to a sequence of one or more N-bit instructions, and then decoding the N-bit instructions.

18. The method of claim 17, wherein the N-bit instructions include an N-bit branch instruction, and the step of operating in the first mode includes decoding the N-bit branch instruction to branch to an M-bit instruction having a memory address with a least significant bit set to a first state to switch from the first state to the second state of operation.

19. In a microcomputer structured to execute N-bit instructions, including an N-bit branch instruction, and M-bit instructions, including an M-bit branch instruction, where M and N are integers, and N is greater than M, a method of executing the M-bit instructions that includes the steps of:

emulating each of the M-bit branch instructions with a sequence of one or more N-bit instructions;

emulating the M-bit branch instruction with a prepare to branch instruction that provides a branch address and thereafter the N-bit branch instruction that uses the branch address.

20. The method of claim 19, including the step of providing at least one target address register, and the step of emulating the M-bit branch instruction includes the prepare to branch instruction loading the target address register with the target address.

21. The method of claim 20, the step of emulating the M-bit branch instruction including the step of the N-bit branch instruction reading the target address for the target address.

22. The microcomputer of claim 14, including a plurality of general purpose registers each for storing data in response to one or more of the N-bit instructions.

23. The microcomputer of claim 22, wherein the plurality of general purpose registers each includes 2N bit positions.

24. The microcomputer of claim 22, wherein predetermined ones of the one or more N-bit instructions load data in low-order bit positions of selected ones of the plurality of general purpose registers.

25. The microcomputer of claim 22, wherein first ones of the one or more N-bit instructions load data in low-order bit positions of selected one of the plurality of general purpose registers, and second ones of the one or more N-bit instructions load data in high-order bit positions of the plurality of general purpose registers.

26. The microcomputer of claim 22, wherein predetermined ones of the one or more N-bit instructions load data in low-order bit positions of selected ones of the plurality of general purpose registers with extension of the most significant bit of the data replicated in high-order bit positions of the selected ones of the plurality of general purpose registers.